Dynamic Range Issues of the new BLM system.

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- While it is certainly true that the new BLM system can handle very large DC Losses. The device saturates at about 50 uA, which corresponds to 715 Rads/Sec or a loss of .014 Rads in 20 uSec. Since we have on average 30nF of cable and 1.5k of switch resistance, we already have an RC of 45 uSec, which gives us a maximum instantaneous loss of .0321 Rads.
- It appears that this instantaneous loss limit is too small, so what can be done to improve this.
  - First we can reduce the bandwidth by increasing the resistance in series with the switch to the integrator.
  - Second we can increase the integrating Capacitor from its current 100pF
  - Finally we can integrate over a shorter time period.

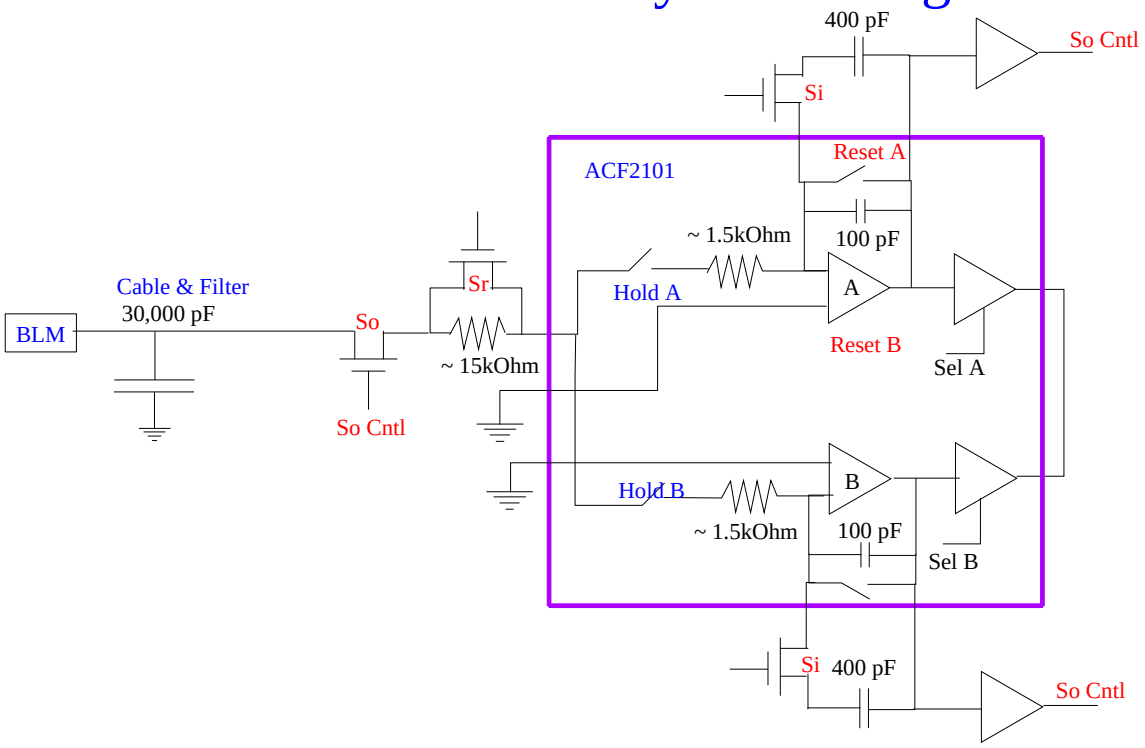
I will deal with the second item first. Using the ACF2101 data sheet's information, I believe that we can safely increase the integration capacitor by a factor of 5. This requires a reset time of 15uSec so it should be OK. This increases the instantaneous Loss limit to about .161 Rads in 20 uSec or 3575 Rads/Sec. The new Max current would then be 250uA, a gain of a factor of 5. In the diagram this capacitor is switched into operation by closing FET Switches labeled Si

The First Item, increasing the series resistance, has the effect of spreading the loss over more time slices. If we assume a cable capacitance of 30 nF. If we assume we increase the RC time to be large compared to the integration cycle, then for the first integration cycle the current is approximately a constant. $I = Q/(R*Ccable)$. If we assume an RC of 500uSec then since Imax=250 uA and RC = 500 uSec, we find a Qmax of 125nC or 1.786 Rads in a 20uSec interval for an additional gain of a factor of 11. In the diagram this resistor is switched into operation by opening FET switch labeled Sr.

Finally, by adding a comparator and S/H, we can look at the integrator's voltage at 1/128, 1/64, 1/32, 1/16, 1/8, and ¼, of a sample period. If at any one of these times the Vint is greater that .4V, then at the next tick we could open the integrators switch to latch the result and ADC the voltage and then bit shift to effectively multiply the value by 64, 32, 16, 8, 4, or 2. This would give us a gain of a factor of 64 so that Imax would be 16 mA. The Max loss in a single sample would then be 114 Rads.

Alternately, we could simply stop integrating by opening the integrator's switch (FET switch So in the diagram) when the voltage on the integrator reaches 10 V (or 9.5V) and just let the cable charge up, we would then keep cycling the integrators until the cable is discharged. This does not require any bit shifting, or precise fractional cycle period timing, and does eventually get all the loss, but at a slower rate, although the timing of the initial loss is precise. Allowing the cable to charge to 100V, a loss of 43 Rads, would then require 12 mSec to fully readout and integrate. While this takes longer to get the full loss, it is simpler to implement and still keeps the time resolution of the start of the loss.

BLM Frontend Mods for Dynamic range Increas



If we implement this plan we may need to do 2 things. We may need an external switch So to stand off the cable voltage, and we may need to keep taking data for 20 to 30 mSec after an abort to be sure we measured all the loss.